

Compal Confidential

Model Name : Bellemere\_BE  
Compal Project Name : B5W1E  
File Name : LA-D121P

# Compal Confidential

## B5W1E Schematics Document

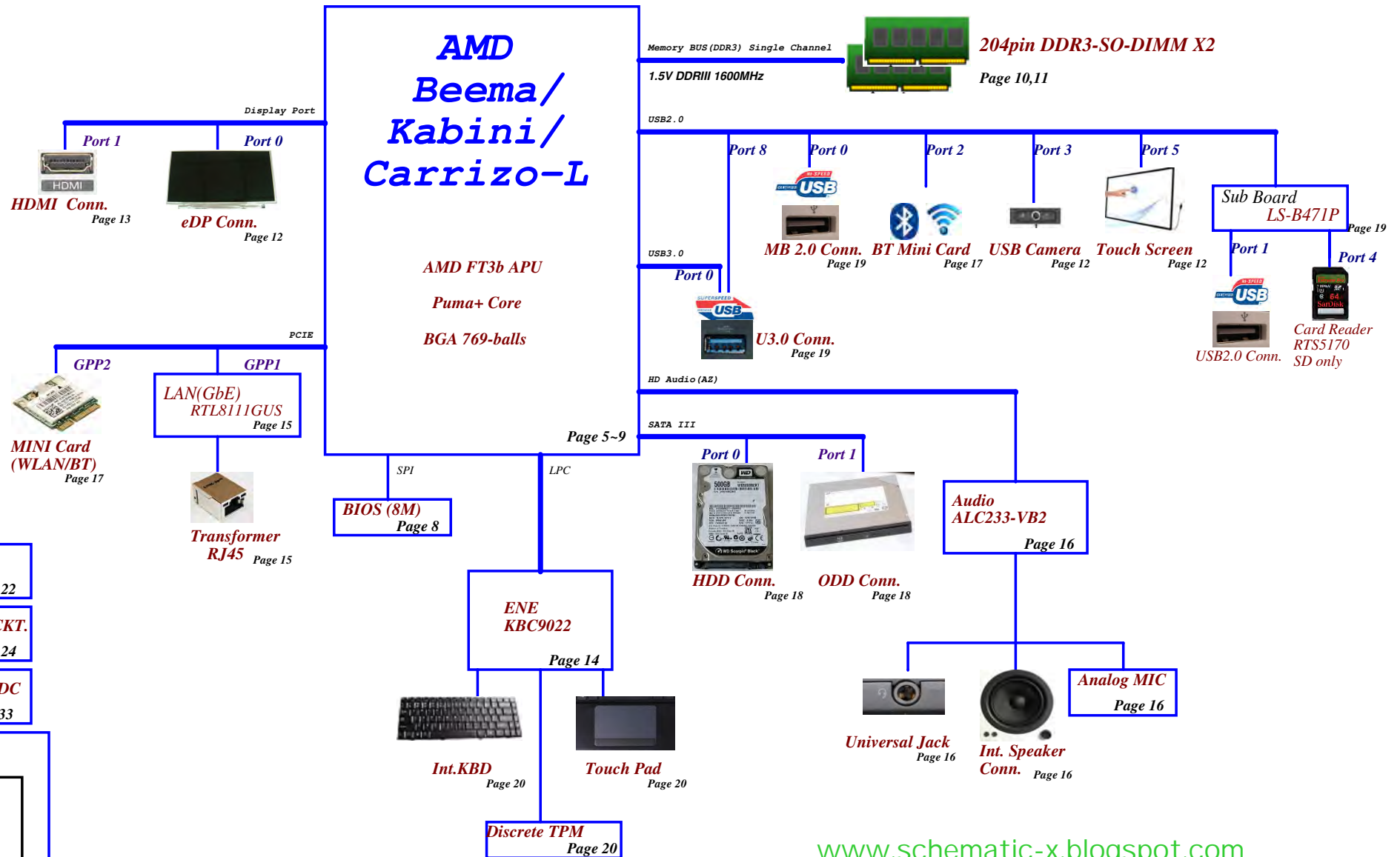
AMD "Beema" Platform  
AMD 15W APU With Puma+ Core

LA-D121P REV: 1.0  
2015-04-16

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/03/27	Deciphered Date	2016/03/27	Title	COVER PAGE	
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				Date	Tuesday, April 21, 2015	Sheet 1 of 33

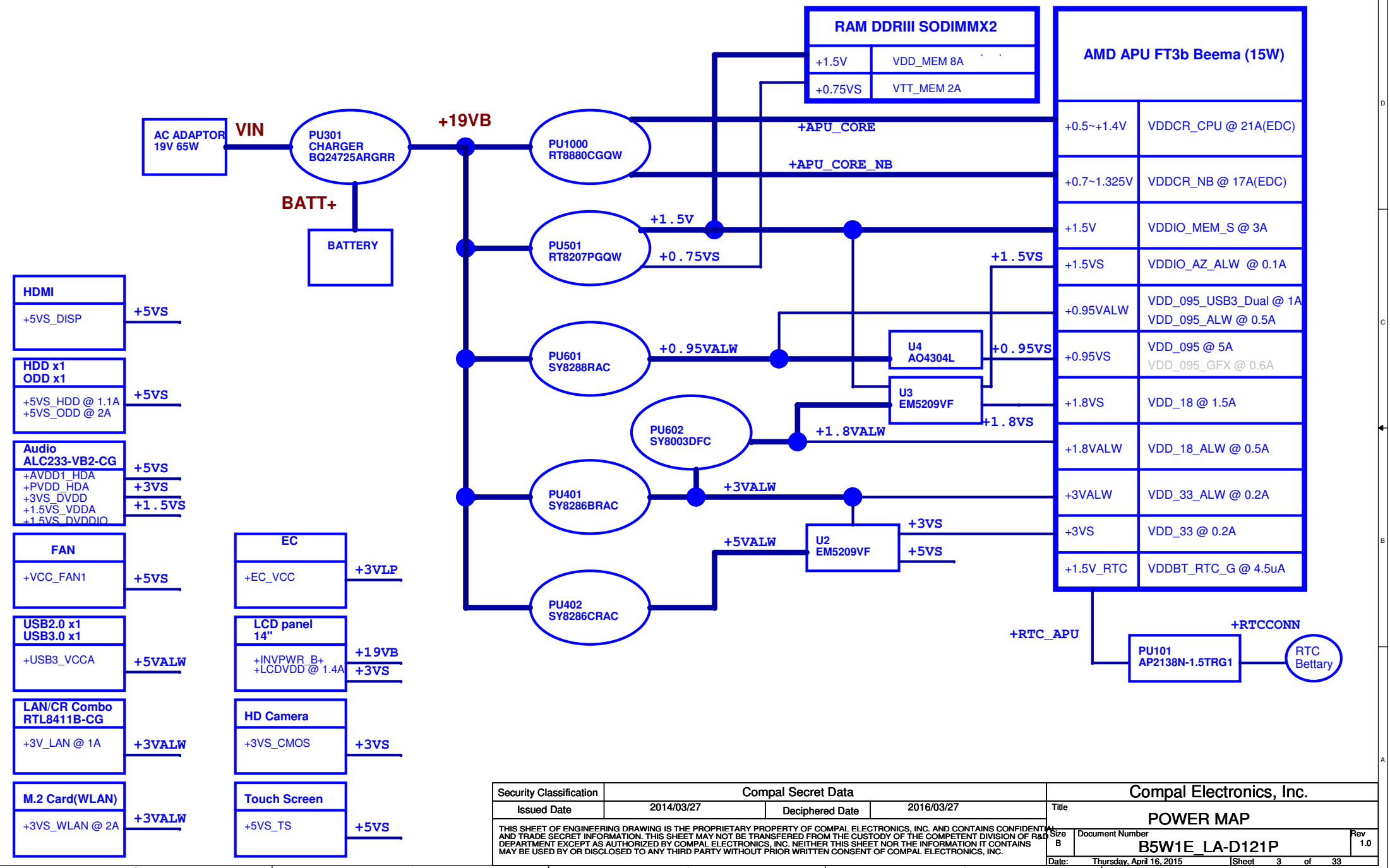
# Compal Confidential

Model Name : B5W1E  
B5W1K  
B5W1R



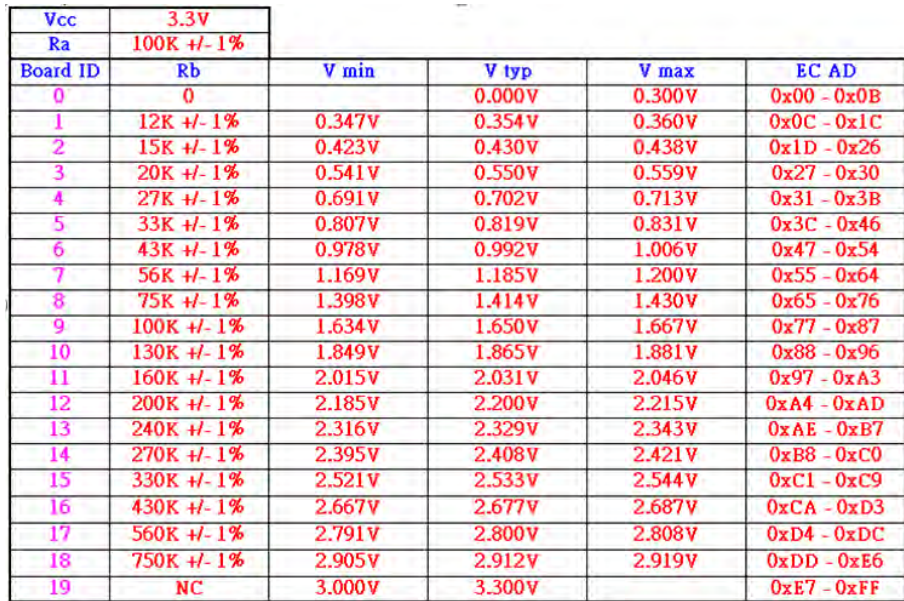
[www.schematic-x.blogspot.com](http://www.schematic-x.blogspot.com)

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[illegible]

EC SMBus Port1 (+3VALW)			EC SMBus Port2 (+3VS)		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	SB-TSI (APU)	1001 100X b	98H



BOM Structure	BTO Item
@	Unpop
CONN@	Connector part control by ME
KBN@	Stuff when use Kabini APU
BMA@	Stuff when use Beema APU
CZL@	Stuff when use CZ-L APU
233@	Use for Audio Codec ALC233-VB2
255@	Use for Audio Codec ALC255
283@	Use for Audio Codec ALC283
EMC@	EMI pop component
@EMC@	EMI unpop component
SP@	Short pad for clear CMOS
HDT@	HDT+ for test phase, MP remove
RS@	R-short
45@	HDMI royalty
9012@	Use KBC9012
9022@	Use KBC9022
BL@	Keyboard backlight
TPM@	Use discrete TPM module
ECI2C@	Use EC I2C T/P
TPUSB@	Use USB to I2C IC for T/P
BYOC@	Stuff when support BYOC
NBYOC@	Stuff when non-support BYOC
JP@	Jump
TP@	Test point

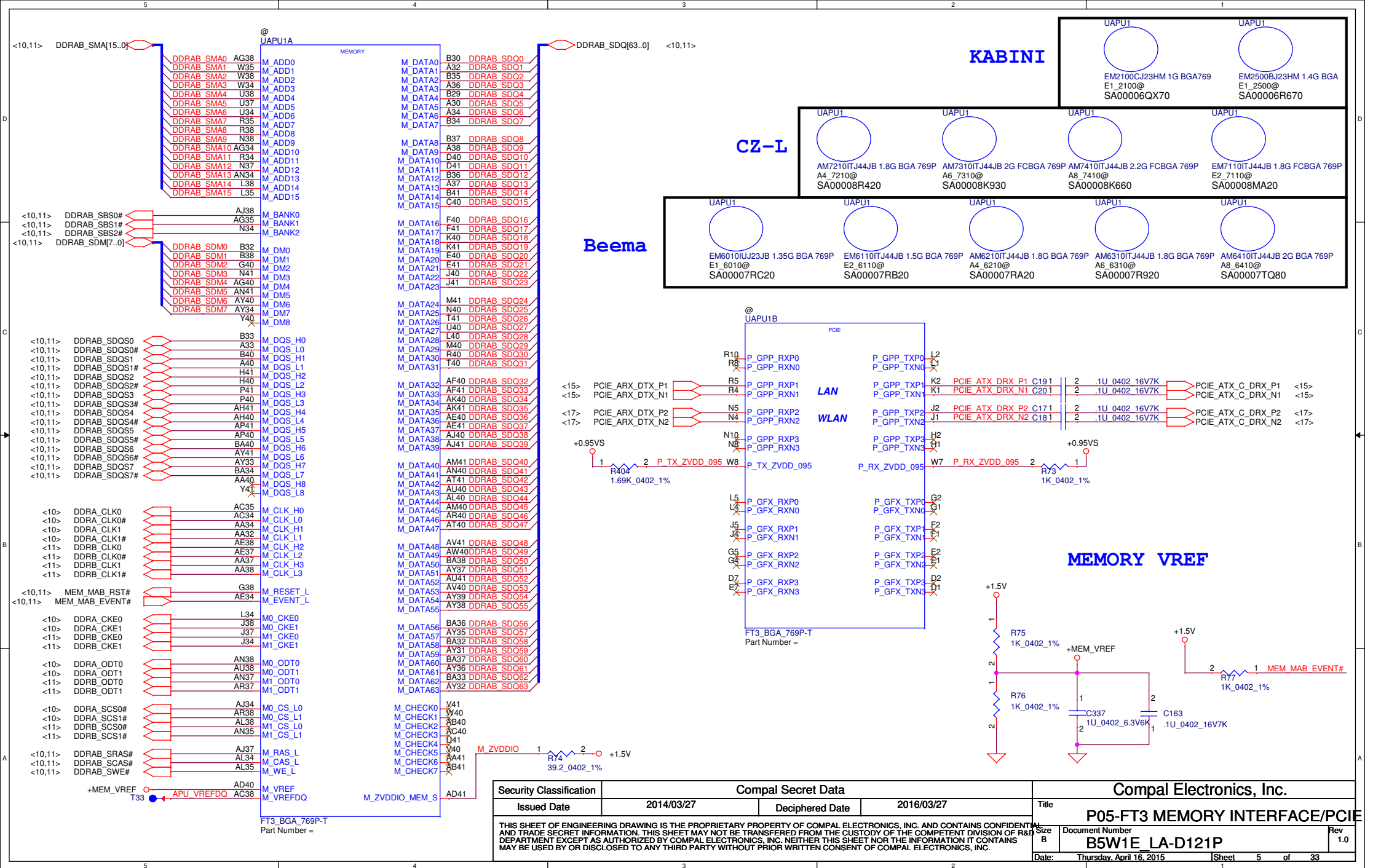
Board ID	PCB Revision
12	EVT
13	DVT
14*	PVT
15	Pre-MP
16	
17	
18	
19	

<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>Full ON</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S1 (Power On Suspend)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>LOW</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

The diagram illustrates the power-up sequence for the ADXL345. The signals and their timing are as follows:

- G-A** (+RTC) and **EC\_ON** are active first.
- G-B** (+3VALW/+5VALW) is active next, followed by **+1.8VALW** and **+0.95VALW**.
- SYSON** is then asserted.
- G-C** (+1.5V) and **SUSP#** are active.
- After a delay, **G-D** (+3VS) is active, followed by **+1.8VS**, **+1.5VS**, and **+0.95VS**.
- VR\_ON** is then asserted.
- Finally, **G-E** (+APU\_CORE) and **+APU\_CORE\_NB** are active.

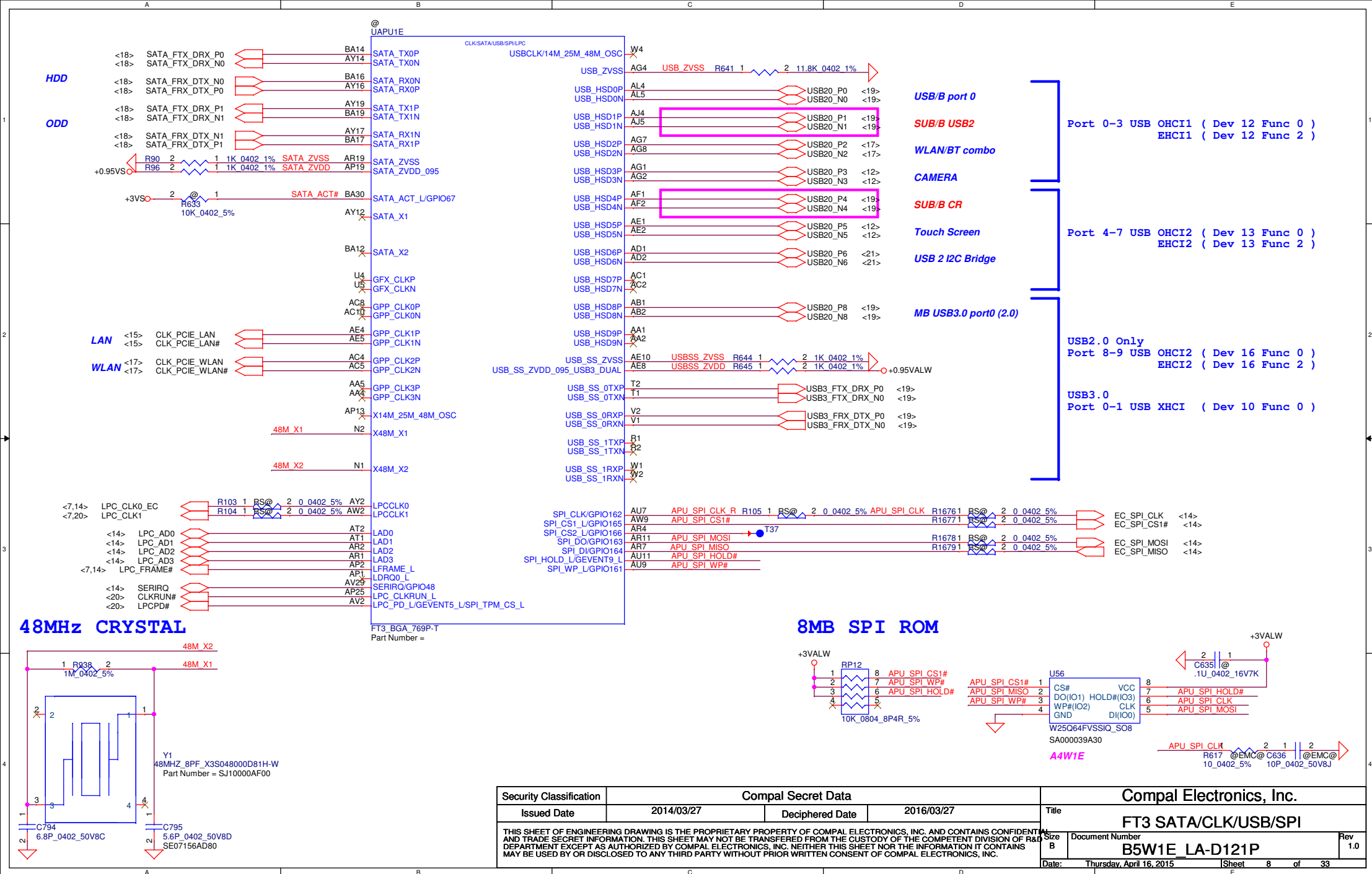
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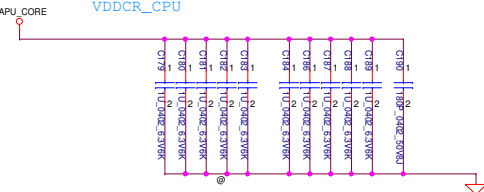




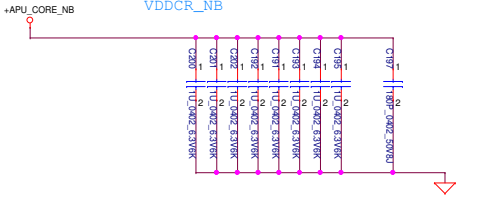




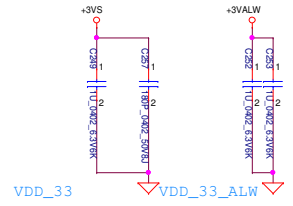
CORE POWER OF APU



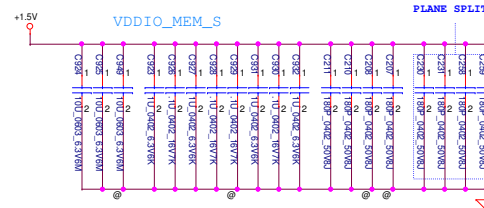
INTEGRATED GPU POWER OF APU



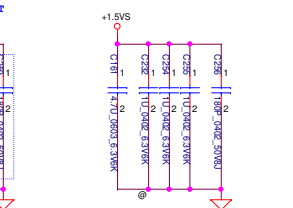
+3VALW/+3VS OF APU



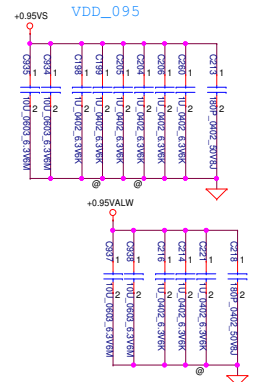
+1.5V/+1.5VS OF APU



VDDIO\_AZ\_ALW (Could be S0 or S5 power rail)



+0.95VALW/+0.95VS OF APU



VDD\_095\_USB3\_DUAL

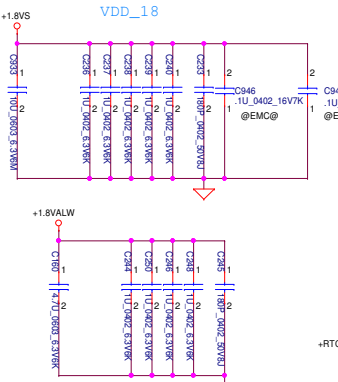


VDD\_095\_ALW

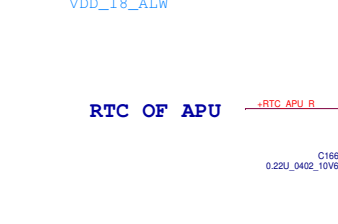
VDD\_18\_ALW

VDD\_18\_ALW

+1.8VALW/+1.8VS OF APU



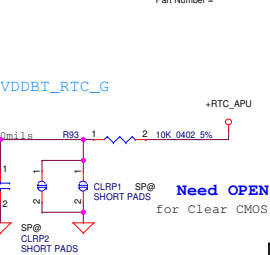
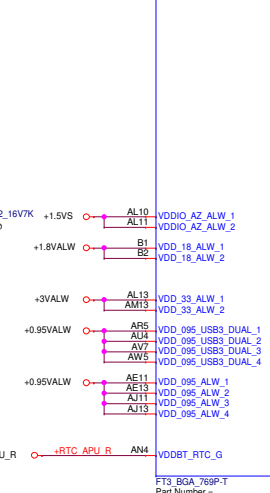
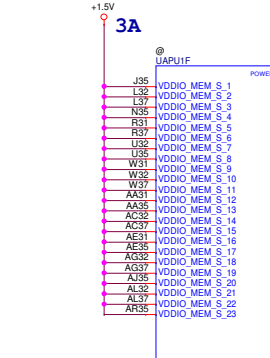
VDD\_18\_ALW



VDD\_18\_ALW

VDD\_18\_ALW

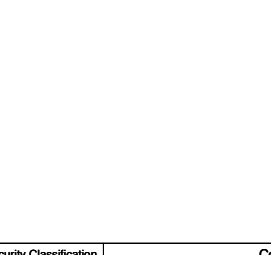
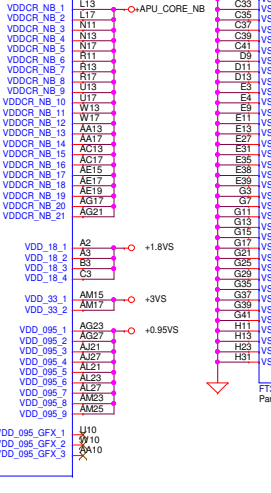
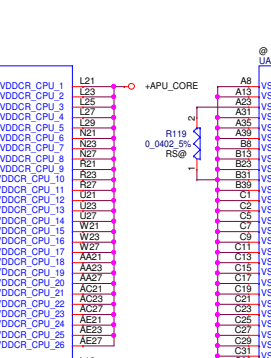
VDD\_18\_ALW



VDD\_095

VDD\_095

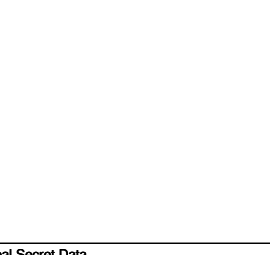
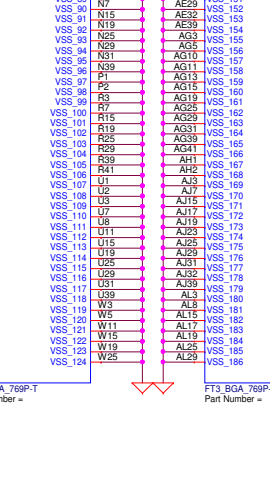
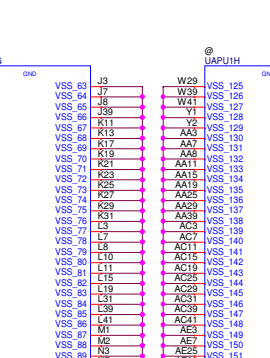
VDD\_095



VDD\_095

VDD\_095

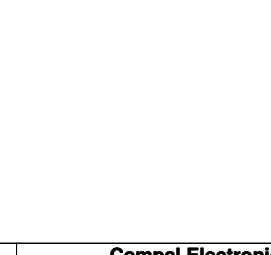
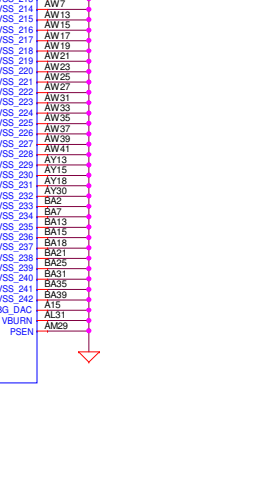
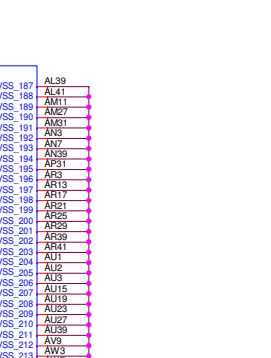
VDD\_095



VDD\_095

VDD\_095

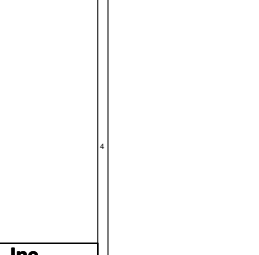
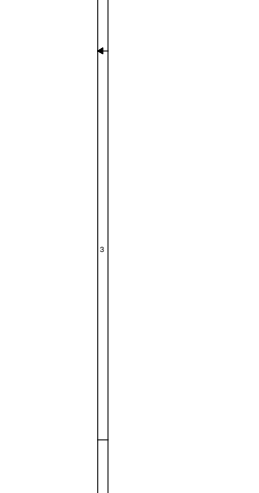
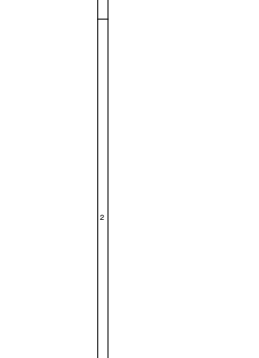
VDD\_095



VDD\_095

VDD\_095

VDD\_095



VDD\_095

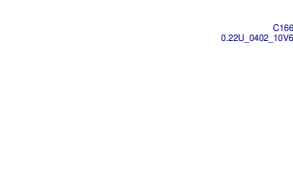
VDD\_095

VDD\_095

RTC OF APU



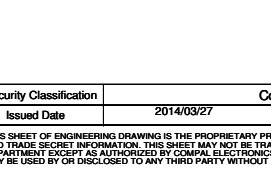
Need OPEN for Clear CMOS



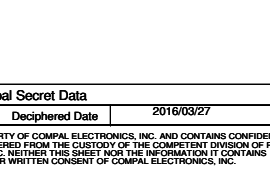
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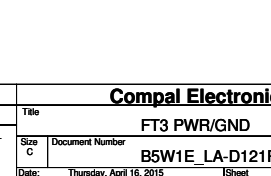
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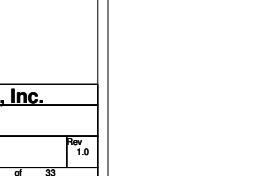
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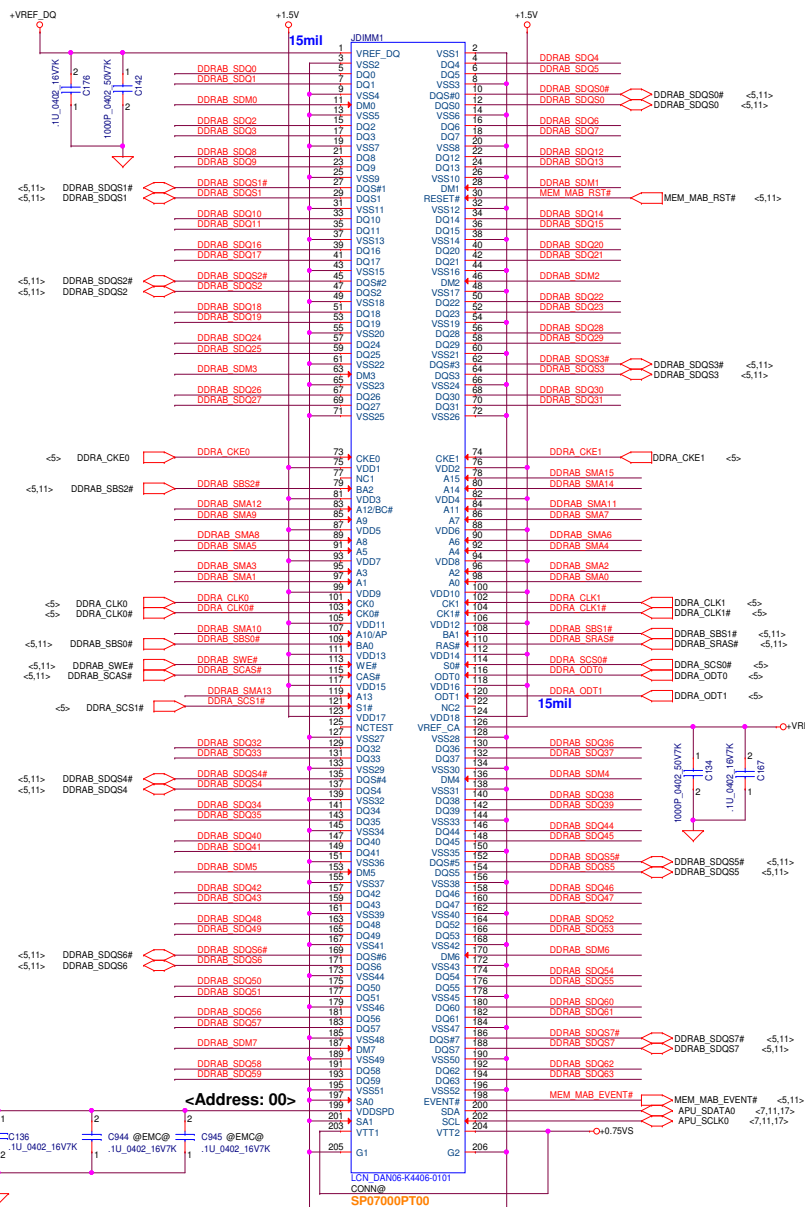
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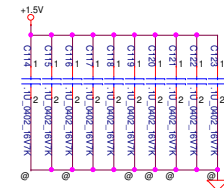
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Title			
FT3 PWR/GND			
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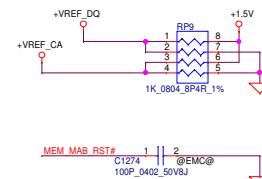
DIMM\_A H:4mm RVS

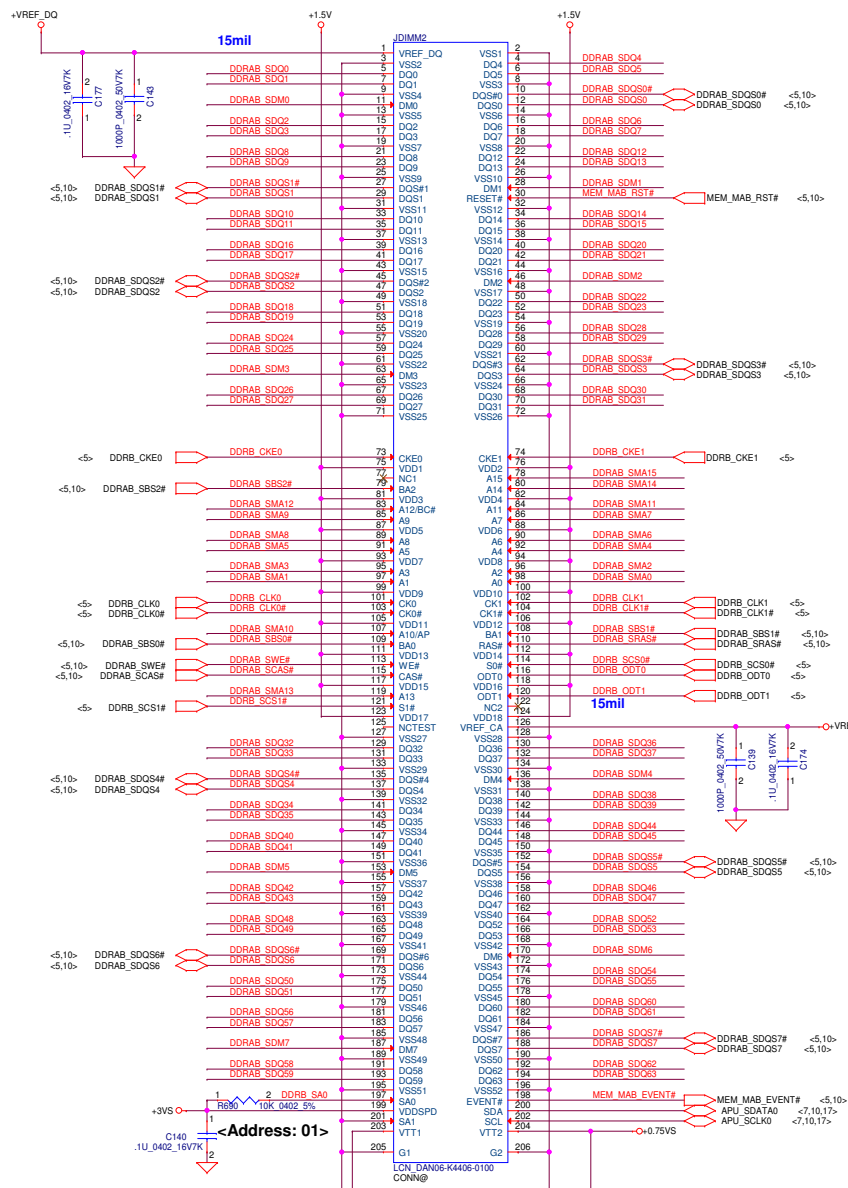
DDRAB\_SDQ0.63V  
DDRAB\_SDM0.7V  
DDRAB\_SMA0.15V

+1.5V/+0.75VS OF DIMM1



VREF for DIMM1,2

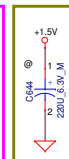
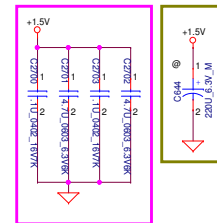
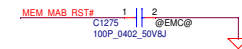
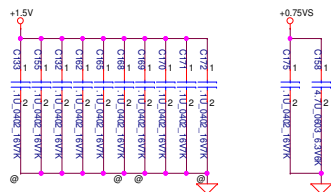




**DIMM\_B H:4mm STD**

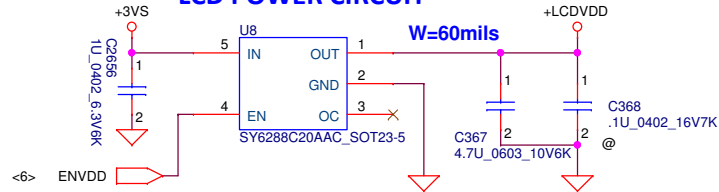


**+1.5V/+0.75VS OF DIMM2**

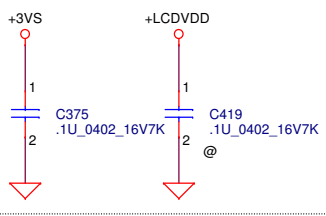


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## LCD POWER CIRCUIT

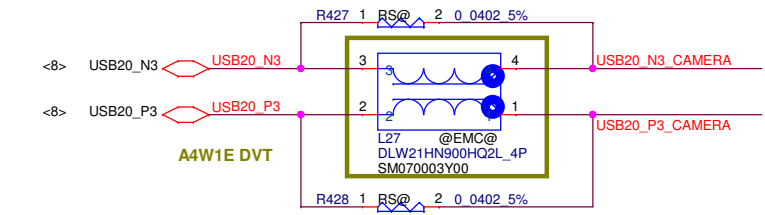
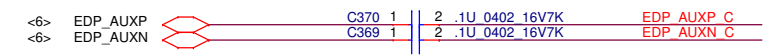
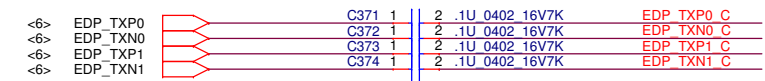
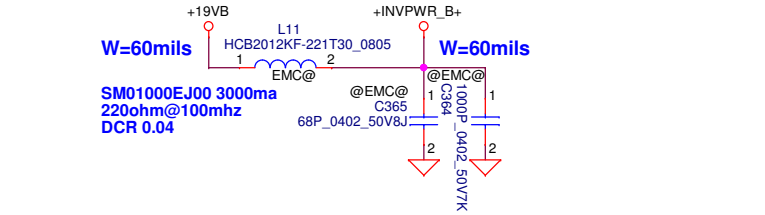
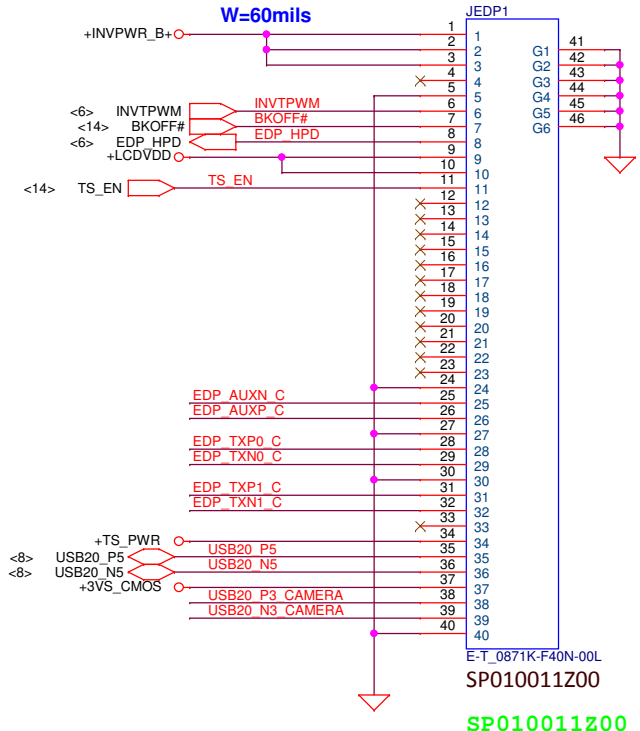


## Place closed to JEDP1

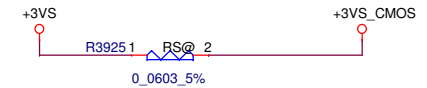
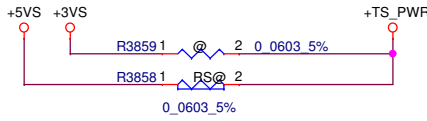


## LED PANEL Conn.

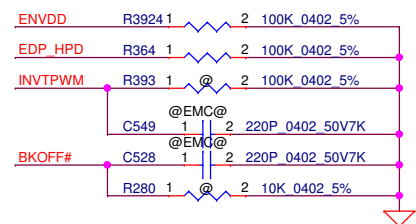
3/13 Change Pin define to follow Z5W1M



Change to R-Short when MP



Touch Screen  
For Camera

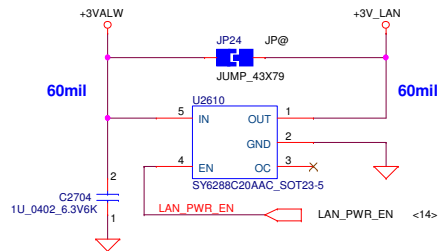


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eDP/Camera/Touch Screen				Document Number
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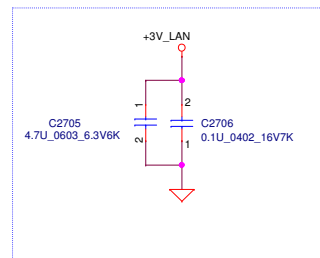




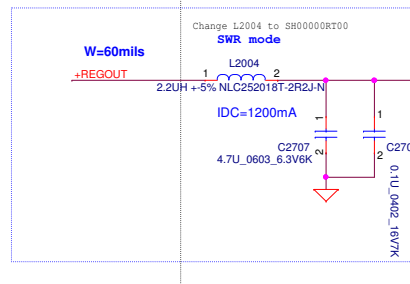




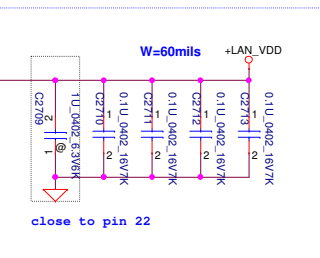
Close to U20 Pin23



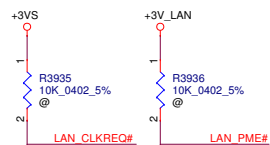
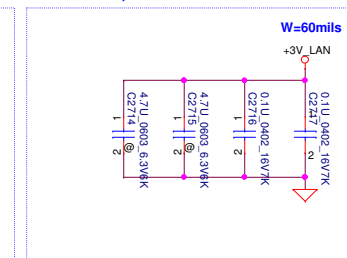
( Should be place within 200 mils )  
Close to Pin 24



Close to Pin 3,8,22,30  
1uF reserved for Pin 22

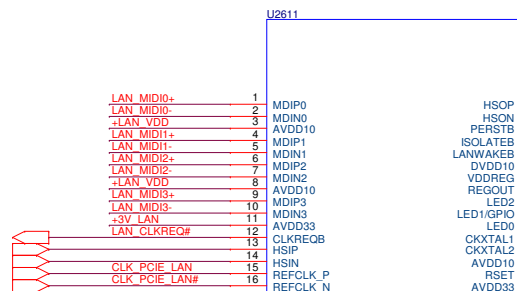


Close to Pin 11,32



PU to +3VS at PCH side

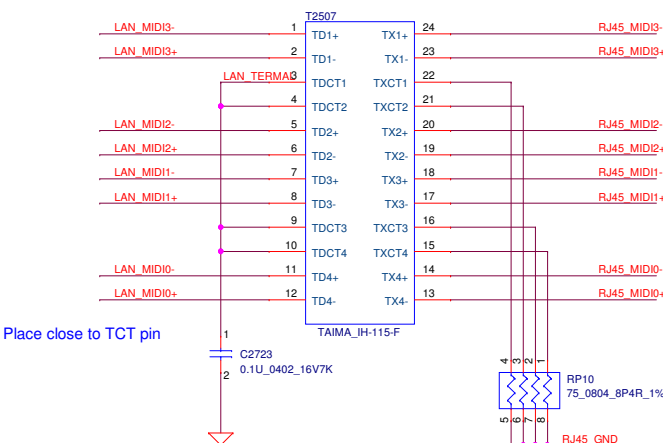
<7> LAN\_CLKREQ#  
<5> PCIE\_ATX\_C\_DRX\_P1  
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RTL8111GS-CG\_OFN32\_4X4

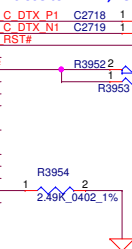
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Use 8111GS symbol , pop 8111GUS part

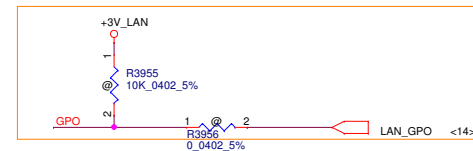


Place close to TCT pin

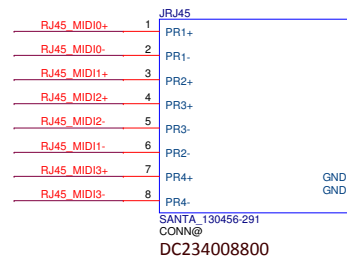
close to Pin 17, 18



EC\_PME# pull high 10K to +3VALW at EC



LAN Connector



40mil

40mil

JUMP\_43X118

JP26

MESC5V02B03\_SOT23-3

EMC@

D201

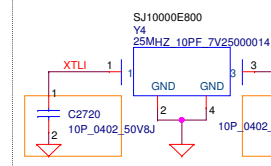
JP27

@EMC@

B88069X9231T203\_4P5X3P2-2

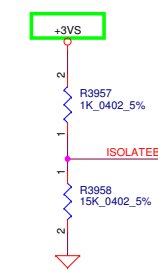
LANGND

LANGND



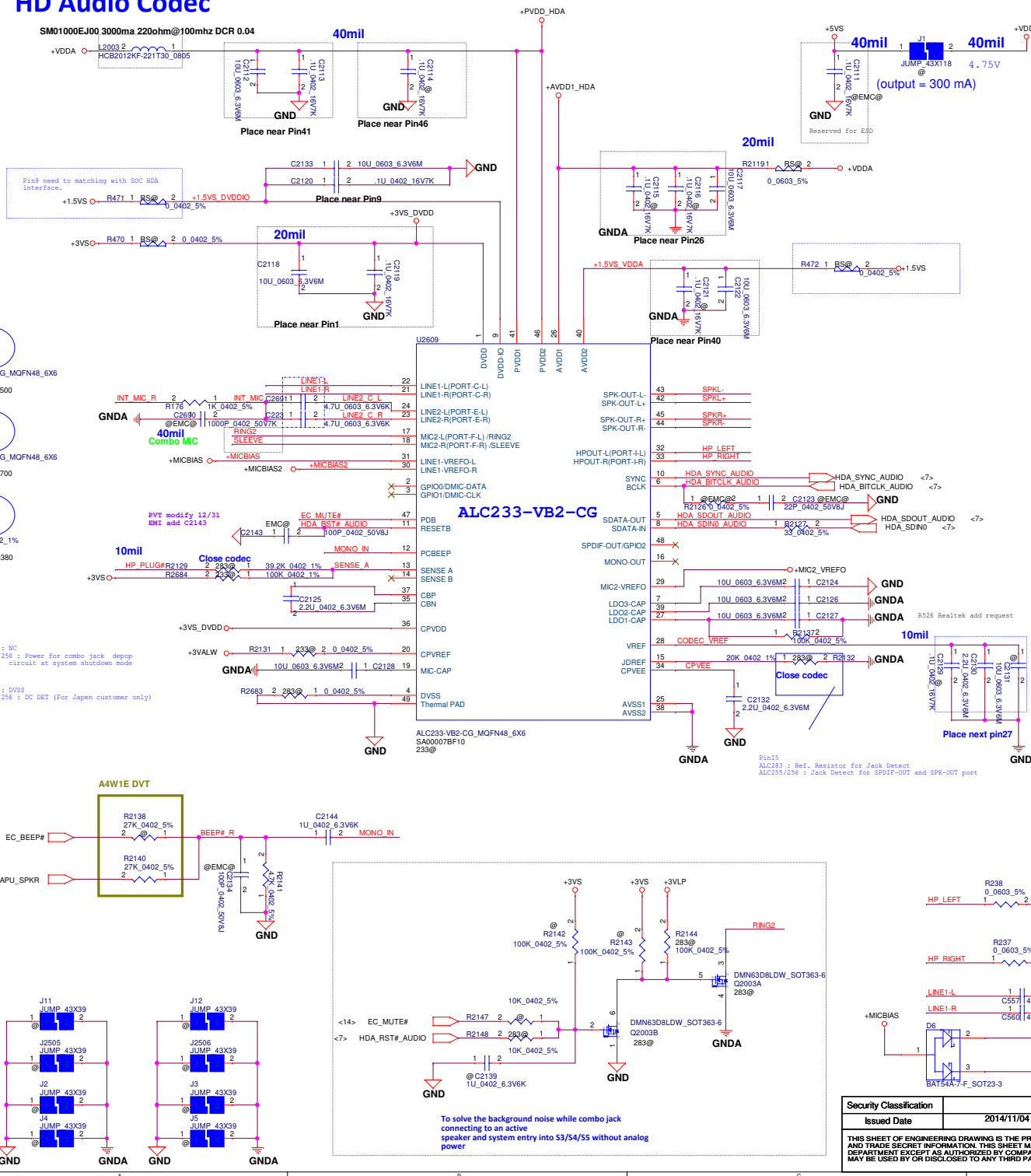
Modify R02

Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S3~S5.

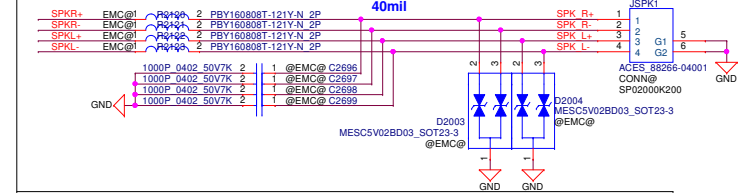


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SA00006ML00				1.0
B5W1E_LA-D121P				15 of 33
Date: Thursday, April 16, 2015				Sheet

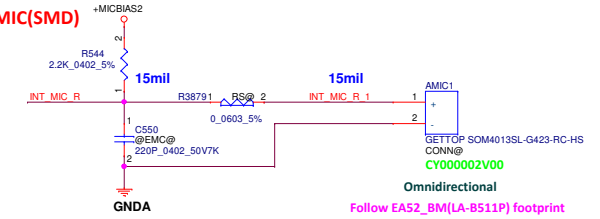
## HD Audio Codec



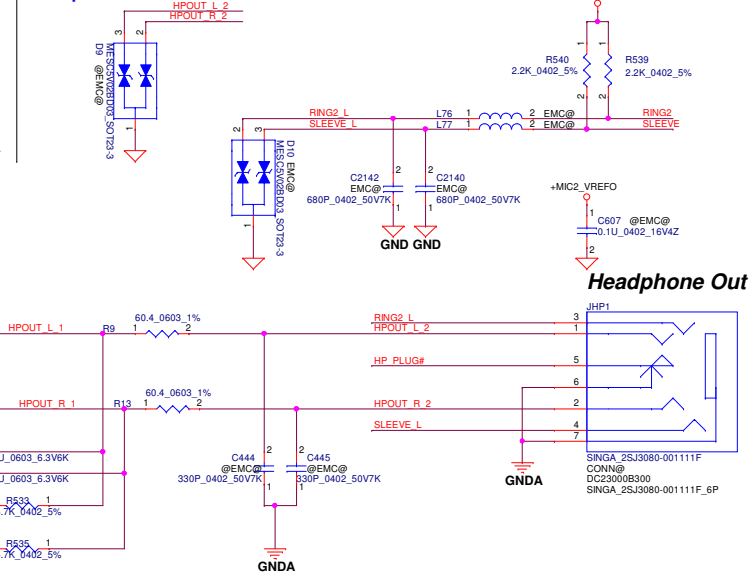
Int. Speaker Conn.



### Analog MIC(SMD)

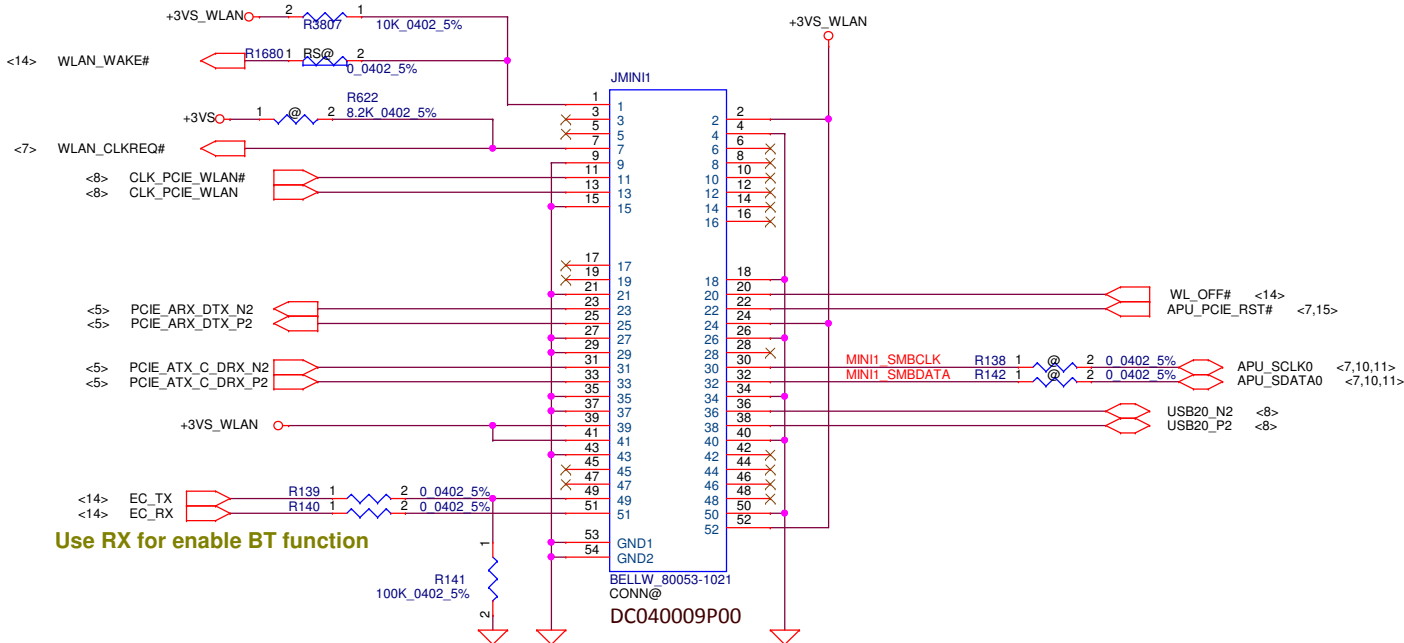
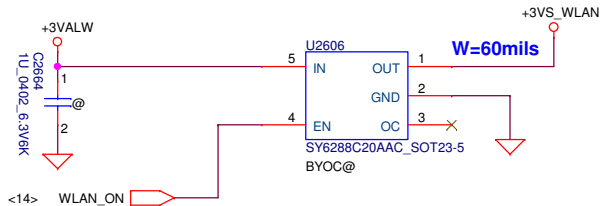
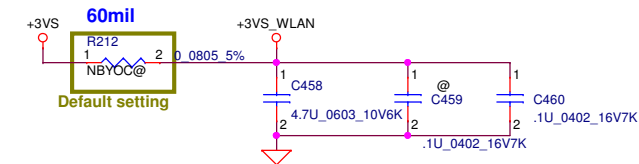


## Headphone Out



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				Date:	Thursday, April 16, 2015	Sheet

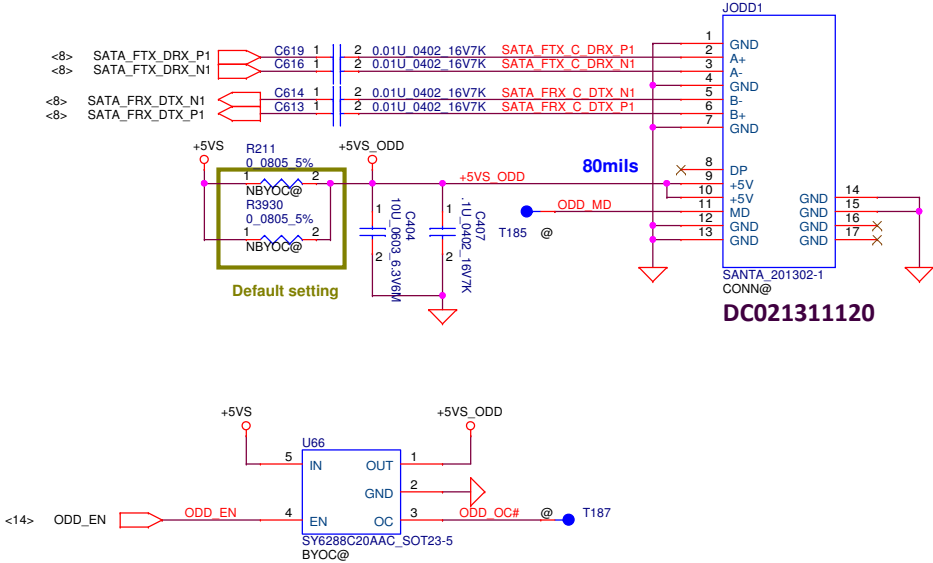
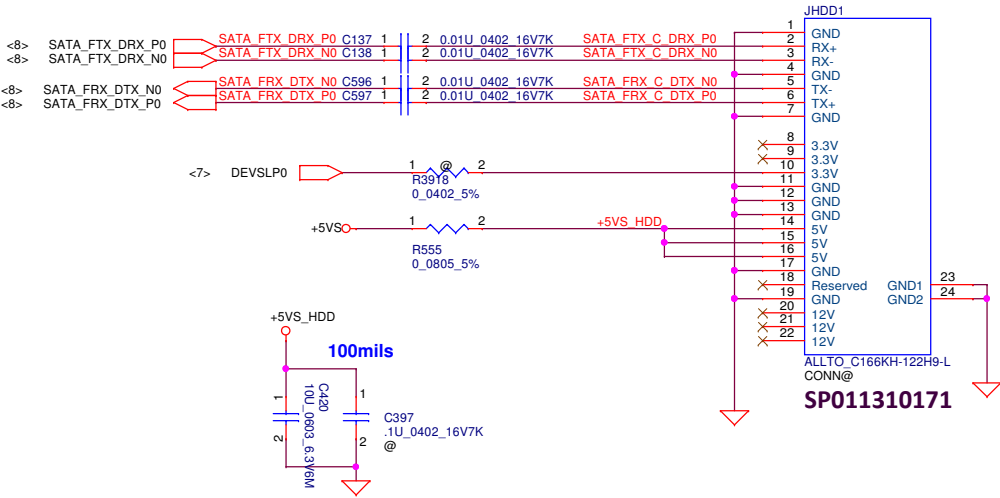
Wireless LAN



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				B5W1E_LA-D121P	1.0
				Date: Thursday, April 16, 2015	Sheet 17 of 33

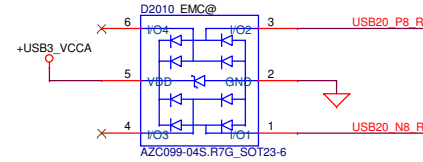
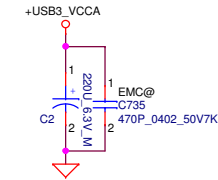
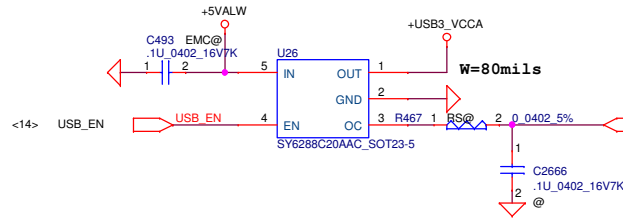
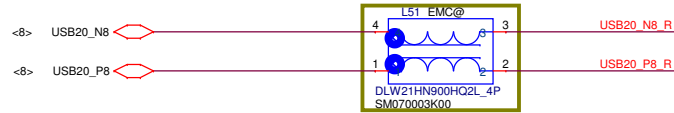
SATA HDD Conn.

SATA ODD Conn.

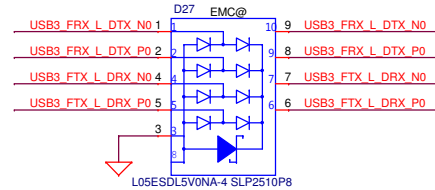


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2014/11/04		2016/11/04		Title	
2016/11/04		Deciphered Date		HDD/ODD	
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B5W1E_LA-D121P		1.0		Date:	
Thursday, April 16, 2015		Sheet		18 of 33	

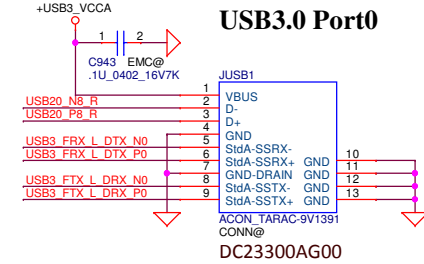
change L51 from SM070003Y00 to SM070003K00



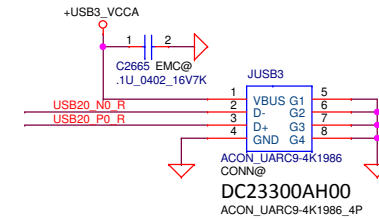
For ESD request



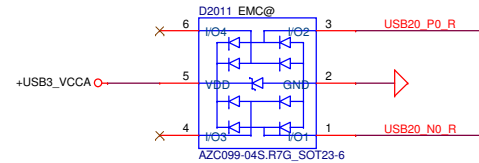
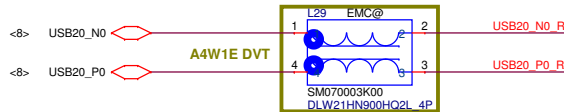
W=80mils



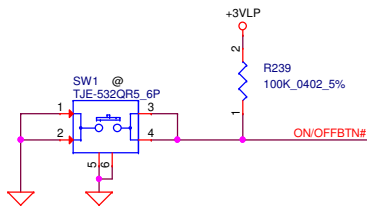
USB2.0 Port0



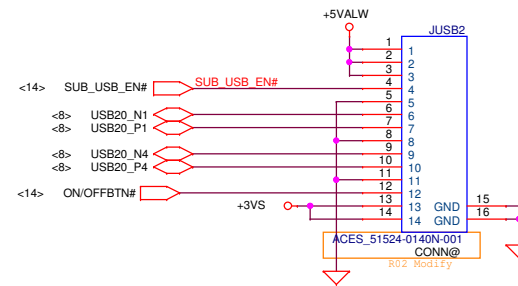
change L29 from SM070003Y00 to SM070003K00



ON/OFF BTN

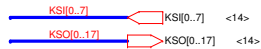


USB & CR/B

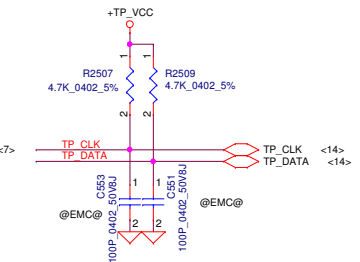
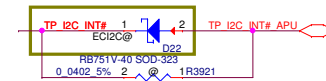


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## KB Conn.



**TP/B Conn.**



### Lid Switch

(Hall Effect Switch)



## TPM Board for 2015



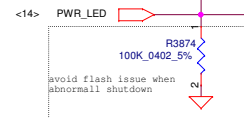
BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh



## LED

**LTST-S115TBKF-CA (SC50000C500)**

**$V_f @ 5 \text{ mA} :$**



UD5: 1.7 ~ 2.3V  
 $(3.3-1.7)/300=5.71 \text{ mA}$   
 $(3.3-2.3)/300=3.57 \text{ mA}$   
 R min: 100 ohm  
 R max 700 ohm

CB5: 2.65~3.05V  
(3.3-2.65)/50=13.00 mA  
(3.3-3.05)/100=5.0 mA  
R min: 50 ohm  
R max:475 ohm

100 1% :SD034100080  
150 1% :SD034150080  
301 1% :SD034301080  
680 1% :SD034680080  
  
120 5% :SD028120080  
560 5% :SD028560080  
200 5% :SD028200080

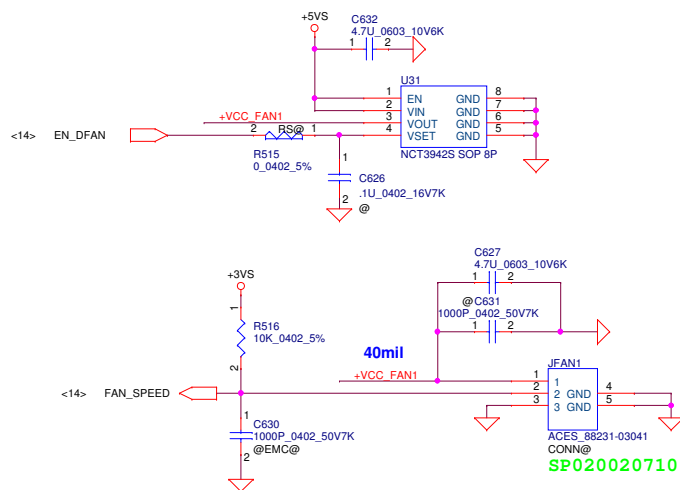


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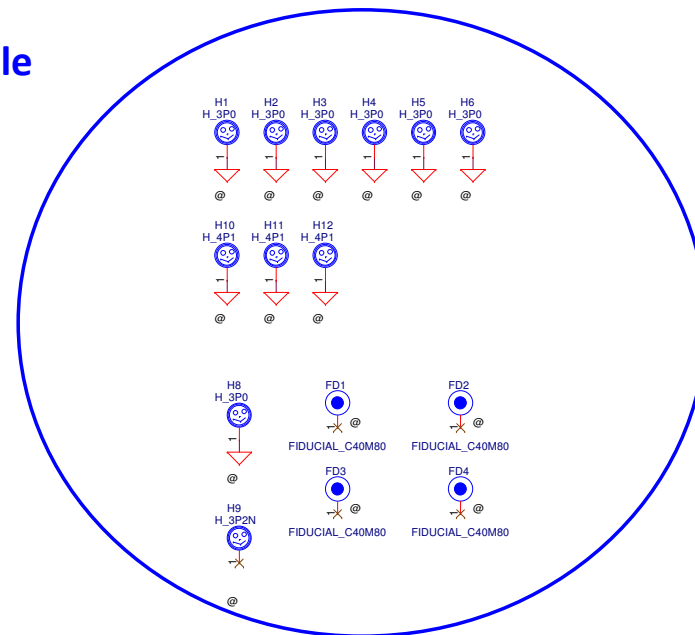




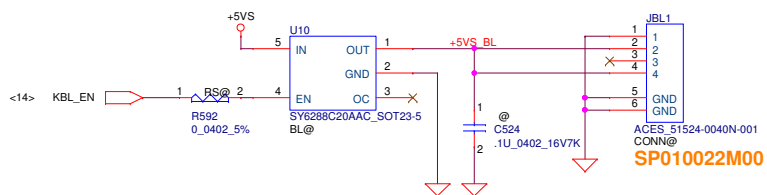
## FAN1 Conn



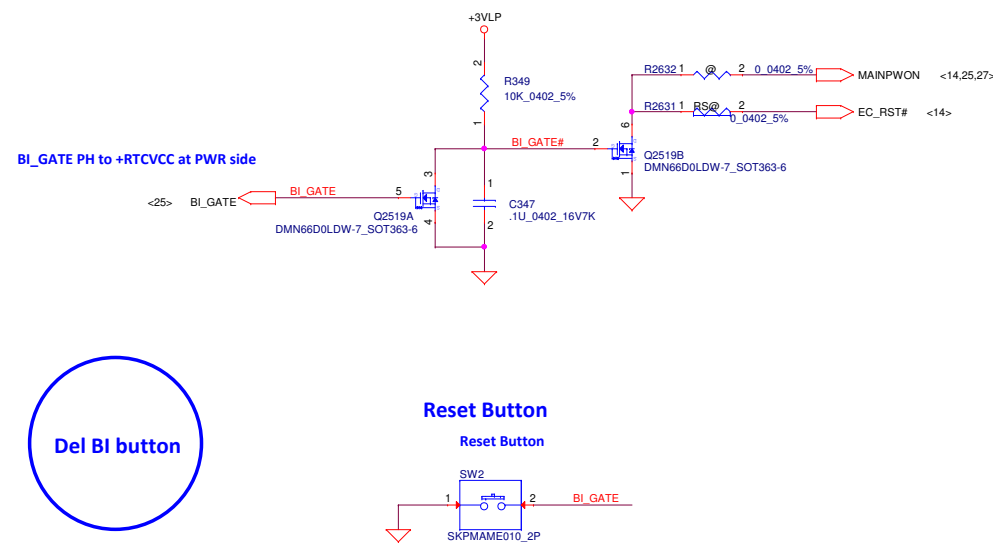
## Screw Hole



## KB BackLight Conn. Reserve

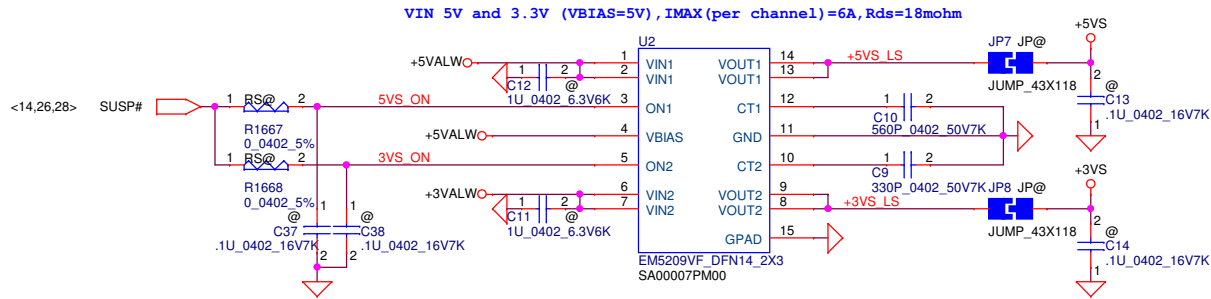


## Reset Circuit

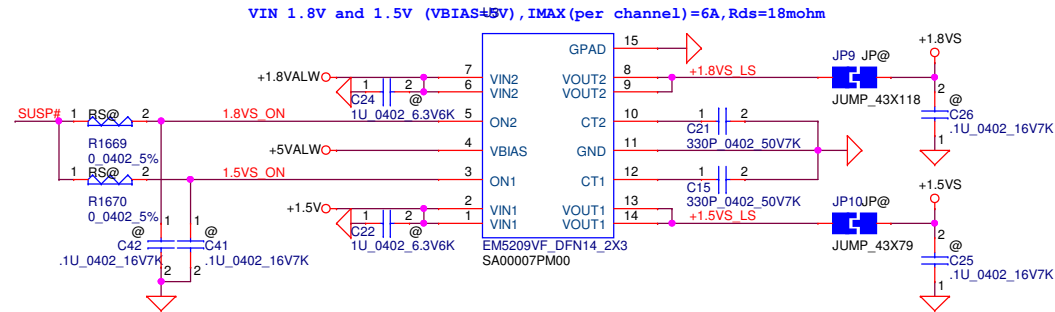


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				Custom	B5W1E_LA-D121P	1.0
				Date:	Thursday, April 16, 2015	Sheet 22 of 33

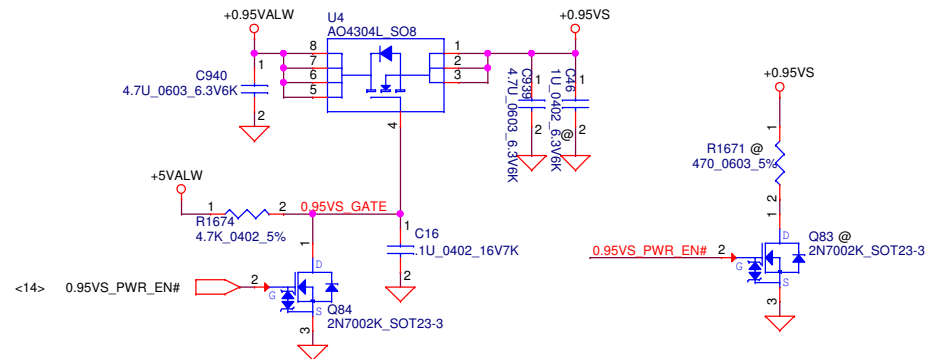
**+5VALW TO +5VS**  
**+3VALW TO +3VS**  
**Load switch**



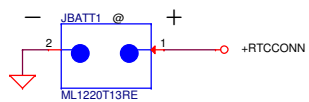
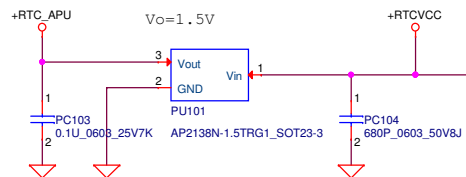
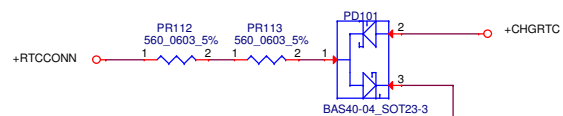
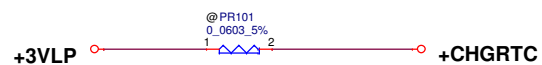
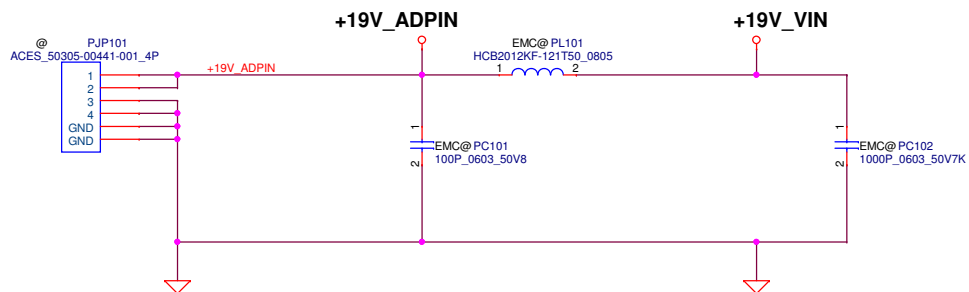
**+1.8VALW TO +1.8VS**  
**+1.5V TO +1.5VS**  
**Load switch**



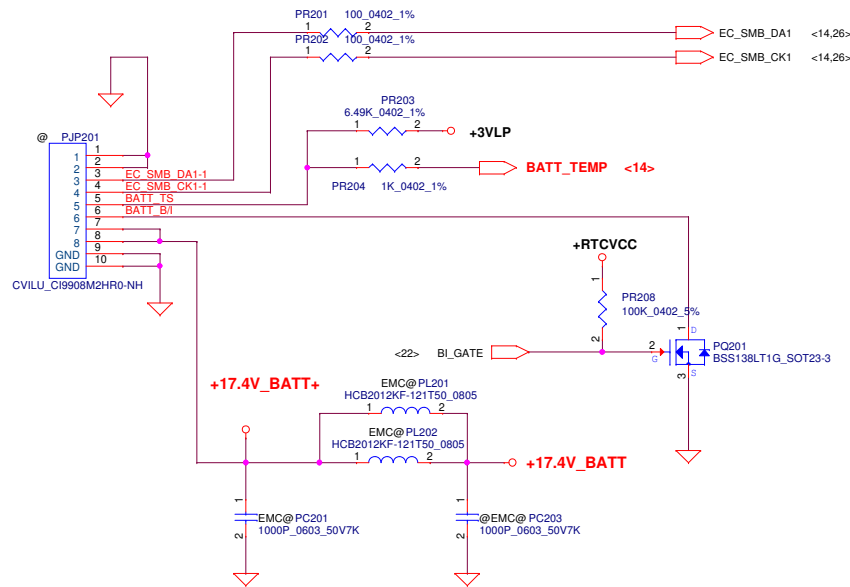
**+0.95VALW to +0.95VS**



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				Date:	Thursday, April 16, 2015
				Sheet	23 of 33



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				1.0
Date: Thursday, April 16, 2015		Sheet 24 of 33		



---Battery\_pin define---

PIN1 GND  
PIN2 GND  
PIN3 SMD  
PIN4 SMC  
PIN5 TS  
PIN6 B/I  
PIN7 Batt+  
PIN8 Batt+

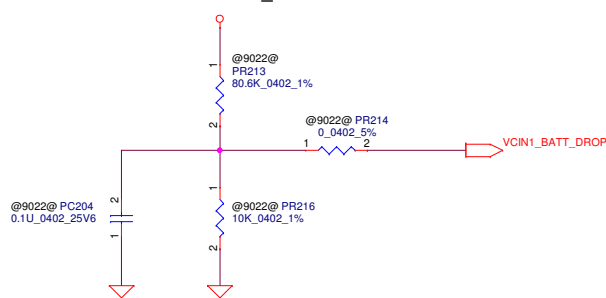
---Battery Con\_pin define---

PIN8 GND  
PIN7 GND  
PIN6 SMD  
PIN5 SMC  
PIN4 TS  
PIN3 B/I  
PIN2 Batt+  
PIN1 Batt+

**2013/10/02**  
**Add for ENE9022 Battery Voltage drop detection.**  
**Connect to ENE9022 pin64 AD1.**

**Reserve for 2-cell design**

**+19VB\_5V**



For 45W adapter==>action 48.15W , Recovery 38.7W

48.15W:  
 $I_{ada} = 0 \sim 2.253A$  ( $48.15W/19V=2.534A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 2.534 * 0.02 = 1.01$   
38.7W:  
 $I_{ada} = 0 \sim 2.036A$  ( $38.7W/19V=2.036A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 2.036 * 0.02 = 0.814$

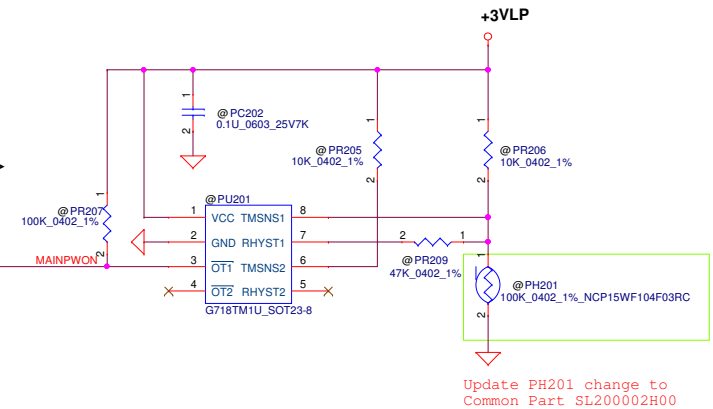
$CP = 45W * 0.85 = 38.25W$

For 65W adapter==>action 69.55W , Recovery 55.9W

69.55W:  
 $I_{ada} = 0 \sim 3.661A$  ( $69.55W/19V=3.661A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 3.661 * 0.02 = 1.464$   
55.9W:  
 $I_{ada} = 0 \sim 2.942A$  ( $55.9W/19V=2.942A$ )  
 $ADP\_I = 20 * I_{ada} * R_{sense}$   
 $ADP\_I = 20 * 2.942 * 0.02 = 1.177$

$CP = 65W * 0.85 = 55.25W$

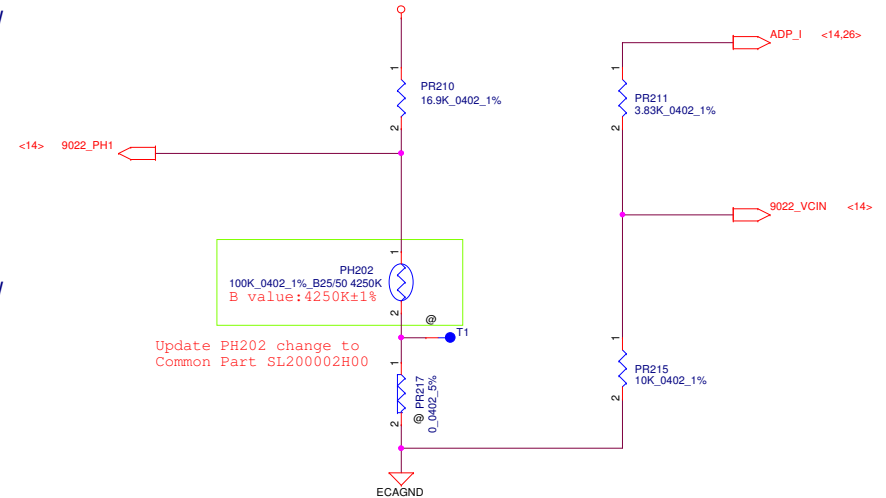
<45, 47>  
<14,22,27> MAINPWON



For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	92C, 1V	56C, 2V
PH202 (ohm)	7.3K	26.11K

For KB9012 sense 20mΩ	Active	Recovery
45W	48.15W, 0.73V	38.7W, 0.59V
65W	69.55W, 0.73V	55.9W, 0.59V

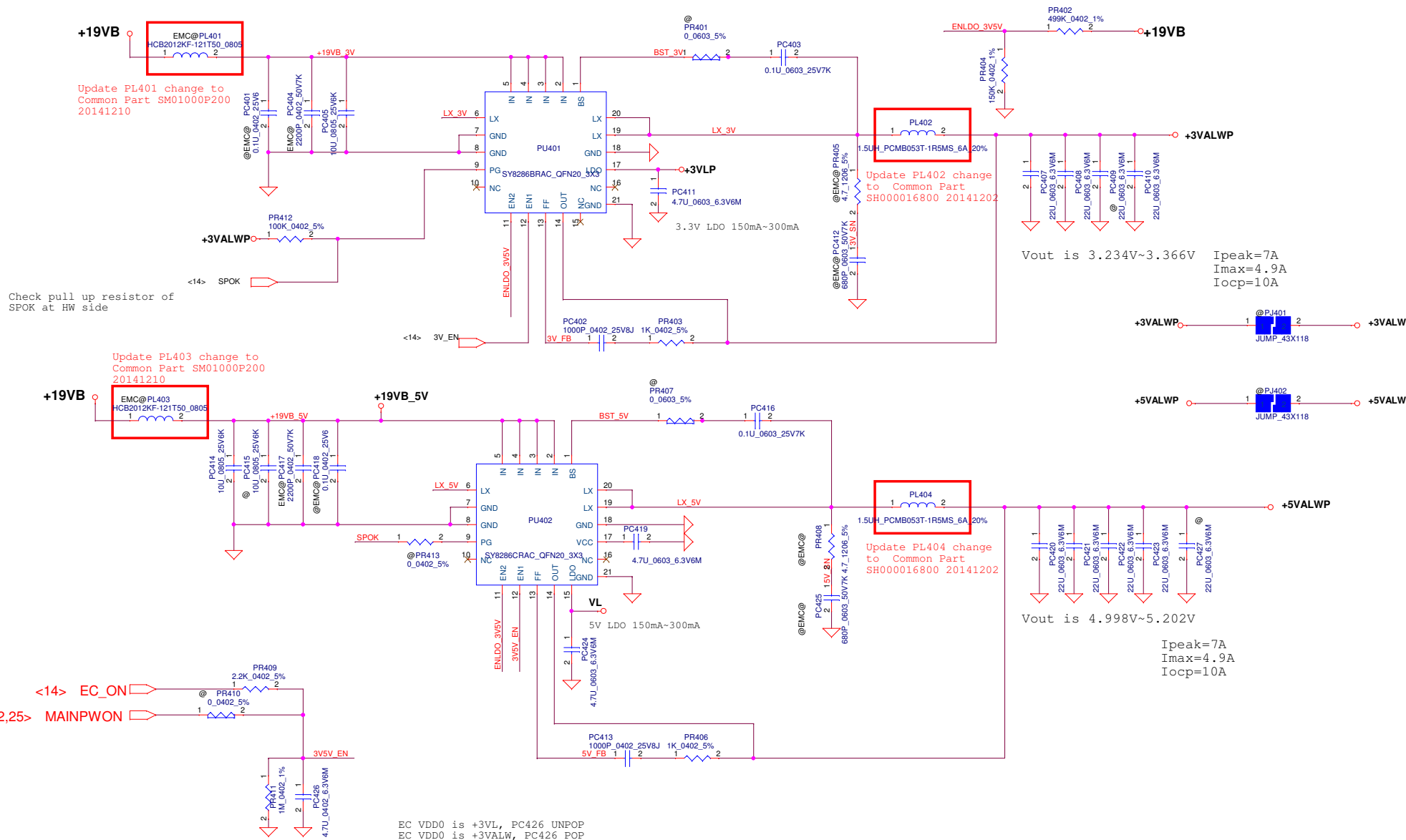
PH202 under CPU bottom side :  
CPU thermal protection at 92 degree C ( shutdown )  
Recovery at 56 degree C +EC\_VCCA



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								Date: Thursday, April 16, 2015				Sheet 25 of 33	

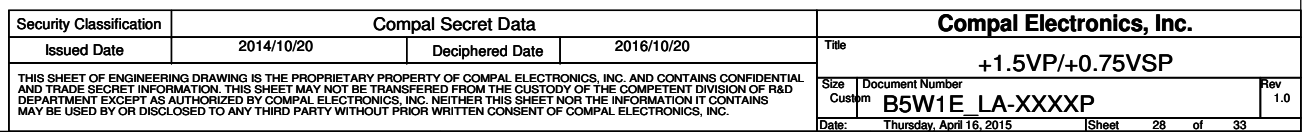


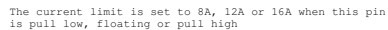




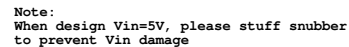
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										Date: Thursday, April 16, 2015		Sheet 27 of 33	

RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer



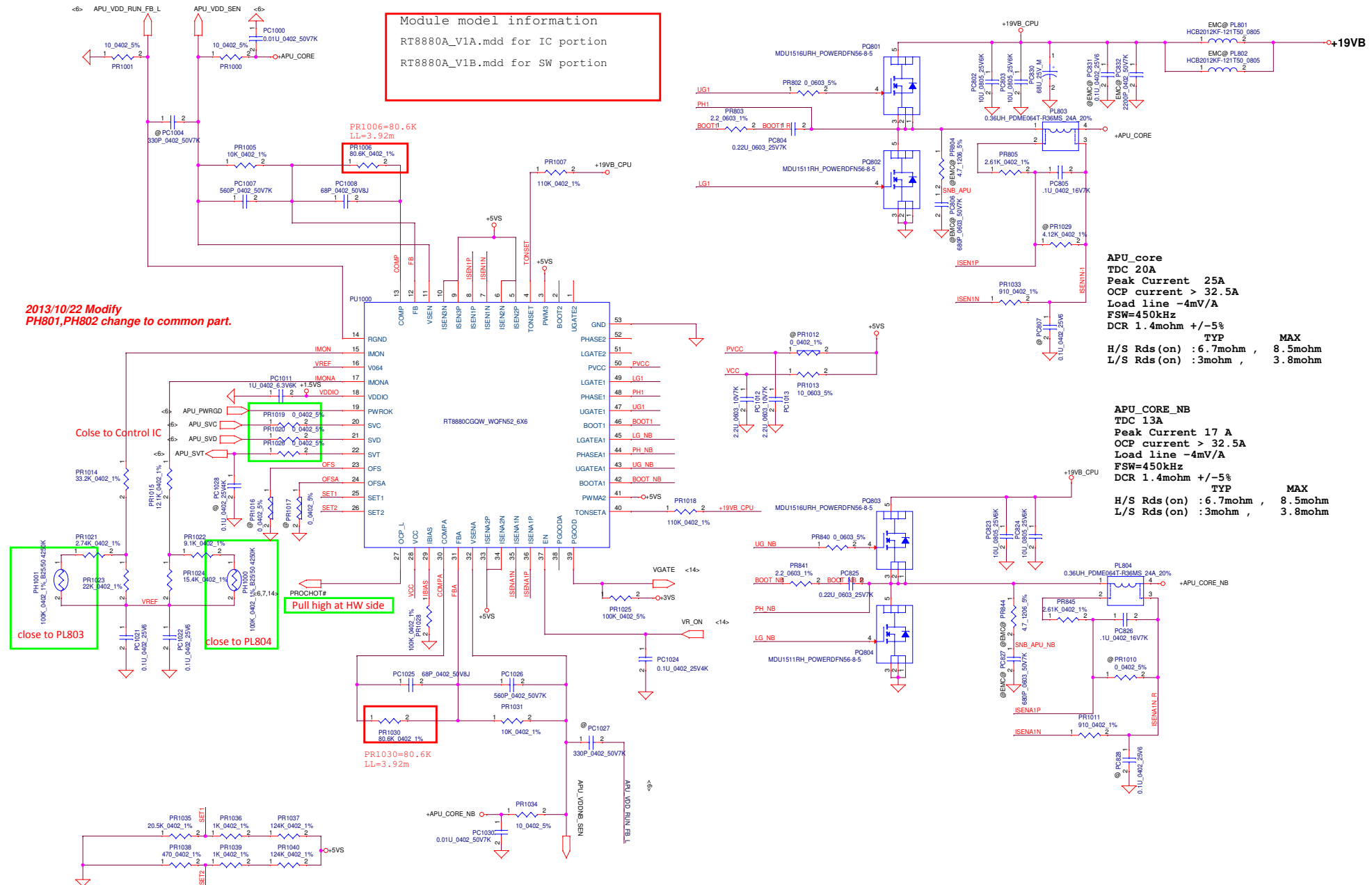


VDDP_ALW_VCTRL	VDDPALW
1	1.062V
0	0.96V



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Issued Date	2014/10/20	Deciphered Date	2016/10/20	Title
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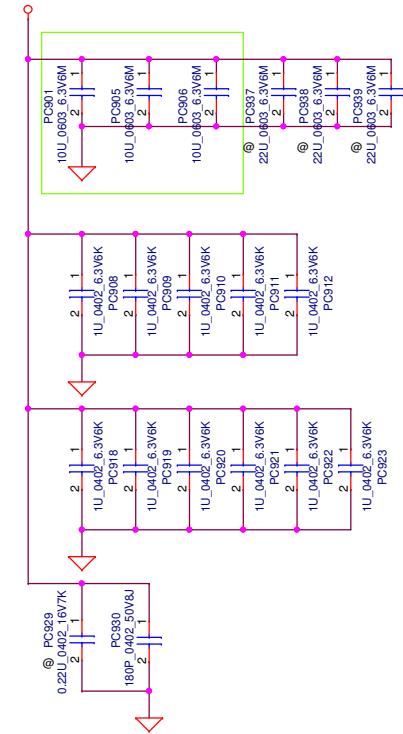
2013/10/16 Modify  
PQ801,PQ803 change to AON6552.  
PQ802,PQ804,PQ805 change to AON6554.



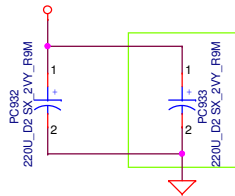
Delete PR834.PR835.PR836.PR839.PR840.PR841,  
follow vender FAE suggest.  
2013/11/29 modify.

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Date: Thursday, April 16, 2015				Sheet	30 of 33

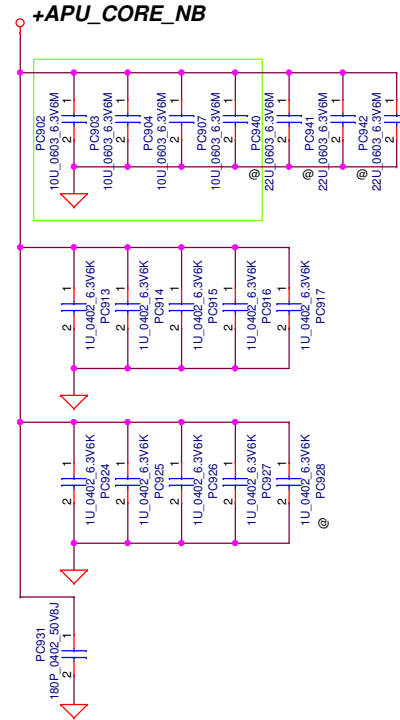
**+APU\_CORE (36.4)**



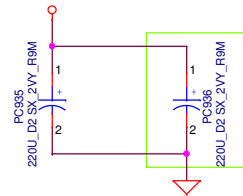
**+APU\_CORE**



**+APU\_CORE\_NB (36.5)**



**+APU\_CORE\_NB**



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